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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,386	11/10/2003	Pierre Liu	2011137	4320

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/705,386	Applicant(s) LIU ET AL.	
	Examiner Quang D. Vu	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: In lines 7-8, the reference numbers should be in the parentheses. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,048,755 to Jiang et al.

Regarding claim 1, Jiang et al. (figures 5-7) teach an integrated circuit package having central leads comprising:

a substrate (56) having an upper surface (a top surface of the substrate [56]), a lower surface (a bottom surface of the substrate [56]), and a long slot (64) penetrating from the upper (a top surface of the substrate [56]) to the lower surface (a bottom surface of the substrate [56]), the lower surface (a bottom surface of the substrate [56]) forming with wiring regions (portions of layer [48]) arranged at the two sides of the long slot (64), and the wiring regions (portions of layer [48]) forming with a plurality of connected points, the length of the wiring regions (portions of layer [48]) are smaller than long slot (64) of the substrate (56);

a resistant layer (a portion of layer is formed near the slot [64] of the substrate [56]) is coated on the lower surface (a bottom surface of the substrate [56]) of the substrate (56), and is located between the long slot (64) and wiring region (portion of layer [48]);

a glue layer (portion of layer [80A]) being coated on the upper surface (a top surface of substrate [56]) of the substrate (56) and being located at the periphery of the long slot (64) ;

an integrated circuit (16) having a first surface (a lower surface of the chip [16]) forming with a plurality of bonding pads and a second surface (an upper surface of the chip [16]), the first surface (a lower surface of the chip [16]) being adhered to the glue layer (portion of layer [80A]), then the bonding pads being exposed from the long slot (64) of the substrate (56);

a plurality of wires (94), each of which is arranged within the long slot (64) of the substrate (56) and is electrically connected the bonding pad of the integrated circuit (16) to the connected point of the substrate (56); and

a first compound layer (portion of layer [92]) being filled within the long slot (64) of the substrate (56) for protecting the each wire (94).

Regarding claim 2, Jiang et al. teach the length of the wiring regions (portions of layer [48]) are shorter than the long slot (64) of the substrate (56).

Regarding claim 3, Jiang et al. teach the connected points of the lower surface (the bottom surface of the substrate [56]) of the substrate (56) is formed with ball grid array (BGA) (balls [88]).

Regarding claim 4, Jiang et al. teach a second compound layer (90), which is covered on the upper surface (the top surface of the substrate [56]) of the substrate (56).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
March 18, 2005

EDDIE LEE
SPE TC 2800